Ampere is leveraging the depth and expertise within the cloud and semiconductor industries to push the boundaries of emerging cloud applications. Our world class team of scientists are focused on the development of new semiconductor designs and building out the first software ecosystem for Arm®-based server processors. We give our customers the freedom to challenge the status quo and accelerate next-generation data centers for the most memory-intensive applications.

Ampere Computing's Headquarters are located in Santa Clara, California, USA. Sales and Engineering offices are located throughout the world.
Vietnam Design Center provides good compensation and benefit programs and working conditions.
Company website: http://www.amperecomputing.com

Please forward resumes to vnjobs@amperecomputing.com

Senior Implementation (Synthesis, Timing) Design Engineer

Job Description:

In this role, you will be responsible for ASIC implementation, including synthesis, floorplanning, timing closure, on our cutting edge ARMv8 based server on chip solutions (X-Gene) that will be the backbone of future data centers. You will be interacting on a daily basis with our design team worldwide and will work on the latest technology (16nm and 7nm) nodes available in the industry.

Responsibilities:

- Responsible for implementation on large state-of-the-art server-SOC blocks, including synthesis, timing constraint generation, timing closure, equivalency checking, and other frontend sign-off.
- Run netlist and physical synthesis on large and medium size blocks.
- Implement and verify other aspects netlist generation like scan-insertion, clock-gating checks, power-domain checks, etc.
- As part of the team, develop front-end implementation flows on synthesis, verification, timing analysis, eco-generation, etc.
- Define timing constraints at block and top level across all modes (Functional / BIST / SCAN / JTAG) and corners.

- Perform timing closure across all corners to ensure successful tapeout following our aggressive deadlines.
- Generate and implement functional ECO.
- Run Logic Equivalent Check (LEC) from RTL to prelayout/postlayout netlist.

Qualifications:

- BS/MS/Ph.D. in Electrical Engineering/Computer Engineering or equivalent and 2-7 years of digital ASIC design/verification experience.
- Experience with Verilog or HDL languages and tools
- Experience in scripting languages (PERL, TCL, shell, etc.)
- Experience in ASIC methodologies and tools like RTL Compiler, Synopsys Primetime, Cadence Tempus, LEC, CDC, etc.
- Physical design experience a plus.
- Timing analysis and synthesis experience a plus.
- Good communication and teamwork skills.
- Good English communications skills, both verbal and writing.

Location:

AMCC Design Center in Ho Chi Minh City, Vietnam.